THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 34

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DANIEL LITAIZE, JEAN-CLAUDE SALINIER, ABDELAZIZ MZOUGHI, FATIMA-ZAHRA ELKHLIFI, MUSTAPHA LALAM AND PASCAL SAINRAT

Appeal No. 96-0609
Application No. 08/024,803[1]

ON BRIEF

Before KRASS, FLEMING, and HECKER, Administrative Patent Judges.

FLEMING, Administrative Patent Judge.

DECISION ON APPEAL

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[1] Application for patent filed March 1, 1993. According to appellants, this application is a continuation of Application No. 07/400,113, filed August 14, 1989, now abandoned.

This is a decision on appeal from the final rejection of claims 1 through 21[2]. Claims 22 through 29 have been withdrawn from consideration.

[2] Claim 9 is incorrect in the Appellants' appendix. We have provided an appendix with the correct copy of claim 9.

The invention relates to a multiprocessor system which allows the exchange of information between central memory and processors via cache memory associated with each of these processors. In particular, Appellants disclose on page 13 of the specification that Figure 1 illustrates the multiprocessor system having n processors CPU_1 to CPU_n and a central random access memory RAM. The central memory is connected in parallel to n shift registers, memory register RDM_1 to RDM_n, each having a memory size sufficient to store one block of information. Each processor CPU_n includes a cache memory MC_j. A shift register, processor register RDP_j, is connected by its parallel port to each cache memory MC_j. Each memory register RDM_n is connected by its serial port to the serial port of a processor register RDP_j by a serial link LS_j.

The independent claim 1 is reproduced as follows:

> 1. A multiprocessor system comprising a central memory (RAM) organized in blocks of information (bi), a plurality of processors (CPU_1 . . . CPU_j . . . CPU_n), a cache memory (MC_j) connected to each processor (CPU_j) and organized in blocks of information (bi) of the same size as those of the central memory, a directory (RG_j) and a management processor (PG_j) associated with each cache memory (MC_j), means for communicating addresses of blocks between management processors (CPU_j) and the central memory (RAM), said multiprocessor system

including a set of memory shift registers (RDM_1 . . . RDM_j . . . RDM_n), each

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of said memory shift registers (RDM_j) of said set having a size of one block of information and being conected [sic connected] to the central memory (RAM) so as to enable, in one memory cycle a parallel transfer of a block of information (bi) between said memory shift register and said central memory, the memory shift registers of said set of memory shift registers being independent of each other for simultaneous shifting of blocks of information,

a plurality of processor shift registers (RDP_1 . . . RDP_j . . . RDP_n) each processor shift register (RDP_j) being each connected to the cache memory (MC_J) of a processor (CPU_j) whereby each processor (CPU_j) has

a dedicated cache memory (MC_j) and a dedicated shift register (RDP_j) for parallel transfer of a block of information (bi) between said processor shift register (RDP_j) and said cache memory (MC_j),

a set of serial links (LS_1 . . . LS_j . . . LS_n), each connecting a memory shift register (RDMj) and a processor shift register (RDP_j) for making a private connection between a paired memory shift register and processor shift register (RDM_j, RDP_j) and transferring at a frequency F of at least 100 megahertz blocks of information (bi) between the memory shift register and the processor shift register (RDM_j, RDP_j) autonomously and independently of other registers and other serial links.

The Examiner relied on the following reference:

Moran 4,257,097 Mar. 17, 1981

Claims 1 through 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Moran. Claims 20 and 21 stand rejected under 35 U.S.C. § 102 as being anticipated by Moran.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs[3] and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 19 under 35 U.S.C. § 103, nor will we sustain the rejection of claims 20 and 21 under 35 U.S.C. § 102.

In regard to the 35 U.S.C. § 103 rejection, the Examiner failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the expressed teachings or suggestions found in the prior art, or

[3] Appellants filed an appeal brief on February 9, 1995. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on July 13, 1995. We will refer to this reply appeal brief as the reply brief. The Examiner stated in the Examiner's letter dated August 7, 1995 that the reply brief had been entered and considered but no further response by the Examiner was deemed necessary.

by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied,*** 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

Appellants argued on pages 5 through 7 that Moran failed to teach or suggest "a set of memory shift registers . . . " as recited in Appellants' claim 1, line 9. In particular, Appellants pointed out that the Examiner merely draws a conclusion of obviousness without presenting any evidence that the invention is obvious.

The Examiner states on page 3 of the answer that "Moran did not teach a plurality of memory shift registers independent of each other for simultaneous shifting of blocks of information independent of other shift registers." On the

same page of the answer, the Examiner states that it would have been obvious to one of ordinary skill in the art to provide multiple shift registers in Moran's memory because it would have provided increased performance of Moran's system. On page 8 of the answer, the Examiner further states that one of ordinary skill would have made the modification to allow more data to be transferred. We note that the Examiner did not provide any evidence in the prior art to support the Examiner's conclusion.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

Upon a further review of Moran, we find that Moran teaches in column 16 memory shift registers 1007-1012 that caused a single block of data to be transferred. We agree that Moran fails to teach or suggest,

> a set of memory shift registers (RDM_1 . . . RDM_j . . . RDM_n), each of said memory shift registers (RDM_j) of said set having a size of one block of information and being connected to the central memory (RAM) so as to enable, in one memory cycle a parallel transfer of a block of information (bi) between said memory shift register and said central memory, the memory shift registers of said memory shift registers being independent of each other for simultaneous shifting of blocks of information, . . . a set of serial links (LS_1 . . . LS_j . . . LS_n), each connecting a memory shift register (RDM_j) and a processor shift register (RDP_j) for making a private connection between a paired memory shift register and processor shift register (RDM_j, RDP_j) and transferring . . . blocks of information (bi) between the memory shift register and the processor shift register (RDM_j, RDP_j) autonomously and independently of other registers and other serial links

as recited in Appellants' claim 1. The Examiner failed to show that the prior art suggested the desirability of the Examiner's proposed modification. We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a ***prima facie*** case. ***In re Knapp-Monarch Co.***, 296

F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); ***In re Cofer***, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Therefore, we find that the Examiner failed to establish why one having ordinary skill in the art would have been led to the claimed invention by teachings or suggestions found in the prior art.

We now turn to the rejection of claims 20 and 21 as being anticipated by Moran. It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. ***See In re King***, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and ***Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co***., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

On page 2 of the reply brief, Appellants argue that Moran does not teach a plurality of shift registers as claimed. We note that claim 20 recites "transferring in one cycle of the central memory, the block (bi) from said central memory (RAM) to one memory shift register (RDMj) of a set of shift registers (RDM_1 . . . RDM_j . . . RDM_n) connected to said central memory." Furthermore, we note that claim 21 recites,

> transferring the block (bi) from said associated cache memory (MC_j) to a

> processor shift register (RDP_j) associated with said cache memory (MC_j), transferring on a serial link (LS_j) the contents of the processor shift register (RDP_j) to a memory shift register (RDM_j) of the same capacity, associated with said processor in a set of shift registers (RDM_1 . . . RDM_j . . . RDM_n) connected to the central memory (RAM).

On page 2 of the answer, the Examiner argues that Moran teaches transferring a block from the central memory to one of a set of memory shift registers (1007-1010) connected to central memory. On page 6 of the answer, the Examiner argues that the claim language reads on Moran's system in that there is a plurality of shift registers 1007-1012 with one out of the set being utilized for transmission of information.

As we pointed out above, Moran teaches in column 16 transferring a block of data from central memory (MM) to the memory shift registers 1008-1010. Moran also teaches in column 15 that the other memory shift registers do not store blocks of data for transfer but store control data and addresses that cause the transfer to occur. However, Moran does not teach a set of shift registers in which each shift register stores a block of data between the central memory and

the processor shift register. Thus, Moran does not teach all the limitations as recited in Appellants' claims 20 and 21.

We have not sustained the rejection of claims 1 through 19 under 35 U.S.C. § 103, nor have we sustained the rejection of claims 20 and 21 under 35 U.S.C. § 102. Accordingly, the Examiner's decision is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
STUART N. HECKER Administrative Patent Judge	)

MRF/sld

Appeal No. 96-0609
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Harold H. Dutton, Jr.
8711 Plantation Lane, #301
P.O. Box 3110
Manassas, VA 22110

Shereece

Appeal No. 96-0609
Application No. 08/024,803

APJ FLEMING

APJ

APJ

REVERSED

Prepared: September 15, 2000